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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/243,101	SUSSER ET AL.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59-150* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59-150* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 11/14/2005.

As indicated in Applicant's response, claims 59, 69, 77, 87, 95, 109, 123, and 137 have been amended. Claims 59-150 are pending in the office action.

Claim Objections

2. Claims 69, 87, 109, and 137 are objected to because of the following informalities:

There should be a underscore for the newly added 'the' between "current object," and "execution of said at least one composite ..." as recited in claim 69. For the sake of expediting the prosecution of the case, the deficiency has been raised merely as an objection, whereas this type of informality can qualify as one that befalls the type of noncompliance related to a 'non-compliant' amendment under 37 CFR 1.121.

There is inconsistency between recitation of the preposition 'the' in claims 69, 87, 109, and 137. It is noted that 'the' appears to be missing between "current object," and "execution of said at least one composite ..." in claims 109 and 137 whereas the same phrase limitation in claims 69 and 87 (li. 11, li. 8, respectively) contains such 'the'. The arguments by Applicants as submitted in the above response (as of 11/14/2005) on pg. 19 concerning the informal use of such 'the' do not seem to support the limitations as recited above; and subject matter for this need to be cleared for record of the case; hence, this inconsistency has to be resolved.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Note: 35 U.S.C. § 102(e), as revised by the AIPA and H.R. 2215, applies to all qualifying references, except when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. For such patents, the prior art date is determined under 35 U.S.C. § 102(e) as it existed prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. § 102(e)).

4. Claims 59-61, 63-69, 71-79, 81-87, 89-95, 97, 99-101, 103-115, 117-129, 131-143, and 145-150 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilkinson et al., USPN: 6,308,317 (hereinafter Wilkinson).

As per claim 59, Wilkinson discloses an application software program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions, said instructions comprising codes and operands (e.g. Fig. 5, 12, 18 – Note: stack parameters checking is equivalent to type and reference safe checking prior to instructions execution) residing on a computer-readable medium (*Loadable application A, B*, Fig. 14);

wherein the program can be loaded to and executed (*Loading and Execution control 120*, Fig. 14) by a *Integrated Circuit Card*, i.e. resource-constrained device as claimed (hereinafter RCD),

said instructions previously converted from one class file (e.g. col. 10, lines 30-47; Fig. 5,6);

said conversion transforming one reference of at least one instructions to information in a constant pool (e.g. *main (ref), (V)V ref 42* – Fig. 9) to data inlined directly in at least one operand

or opcode of said instructions (e.g. *V ref* 91, data *FFF3* – Fig. 9 – Note: memory holding place of opcode being inlined directly by a substituted value reads on data inlined directly in at least one operand or opcode),

so that said at least one reference to information in said constant pool is eliminated (e.g. *V/V (ref) 42, FFF3 47* – Fig. 9 – Note: constant FFF3 in address 47 created in line with FOO1 reads on eliminating reference V/V ref in the original constant pool address 42).

As per claim 60, see Wilkinson: Fig. 9 (re claim 59)

As per claim 61, see Wilkinson: Fig. 9 (Note: inlining data into instructions or operands of instructions is implicitly disclosed in Fig. 9).

As per claim 63, see Wilkinson: col. 7, lines 43-56.

As per claim 64, Wilkinson discloses a resource-constrained device having RAM of no more than 64Kbytes (Fig. 1; col. 7, lines 43-56).

As per claim 65, Wilkinson further discloses the RCD having RAM of no more than 4Kbytes (col. 7, lines 43-56).

As per claim 66, Wilkinson further discloses a Java card virtual machine (*Card JVM 16*, Fig. 1), a VM residing on a microprocessor of the RCD.

As per claim 67, see Wilkinson: *Card JVM 16*, Fig. 1; col. 1, lines 16-19.

As per claim 68, see Wilkinson: *integrated circuit* - col. 3, lines 17-24, 51-58; Fig. 1, 21 (note: circuit built for specific application, e.g. Fig. 22, as smartcard implies an application specific IC)

As per claim 69, this claim recites the same limitations as claim 59 which Wilkinson has met as per rejection in claim 59. That is, Wilkinson discloses an object-oriented, verifiable,

type-safe and pointer-safe sequence of instructions, said instructions comprising codes and operands (e.g. Fig. 5, 12, 18 – Note: stack parameters checking is equivalent to type and reference safe checking prior to instructions execution) residing on a computer-readable medium (*Loadable application A, B*, Fig. 14);

wherein the program can be loaded to and executed (*Loading and Execution control 120*, Fig. 14) by a *Integrated Circuit Card*, i.e. resource-constrained device as claimed (hereinafter RCD),

said instructions previously converted from one class file (e.g. col. 10, lines 30-47; Fig. 5,6).

Further, Wilkinson further discloses that said converted instructions comprise at least one composite instruction for performing an operation on a current object (e.g. ILOAD_0, ILOAD_1 – Fig. 7; ILOAD_B – Fig. 11 Note: instructions embedding operands and data which can be decomposed into separate parts of the instructions to be executed are equivalent to composite instructions), the execution of said at least one composite instruction generating a result functionally equivalent to a result generated by operations on said current object resulting from sequential execution of two or more instructions (e.g. col. 10, lines 35-51; refer to Appendix D of US 2003/0023954 by Wilkinson – Note: sequential execution of instructions that would have taken place for achieving what a composite instruction, e.g. ILOAD_x or ALOAD_x, amounts to is disclosed in pg. D-2, D-3 of Appendix D)

so that said sequential execution of said two or more other instructions is replaced by said execution of said composite instruction in said sequence of instructions (Fig. 11; col. .11, lines 24-35; pg. 29, Appendix D-2 of US 2003/0023954 by Wilkinson – Note: sequential instruction

as to load separate operands or integers into a stack along with the ILOAD operand read on sequence of separate load instructions (2 or more) to achieve functionally equivalent result by replaced using composite instruction ILOAD_x – or ALOAD_x, each such stack load instruction reading on instructions to be executed in sequence).

As per claims 71-76, refer to corresponding rejections of claim 63-68, respectively.

As per claim 77, Wilkinson discloses a resource-constrained device (Fig. 2) comprising:

a memory for storing (e.g. *Card ROM 140* -- Fig. 14) an application program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions, said instructions comprising codes and operands (e.g. Fig. 5, 12, 18);

said instructions previously converted from one class file (e.g. col. 10, lines 30-47; Fig. 5,6);

said conversion transforming one reference of at least one instructions to information in a constant pool (e.g. *main (ref), (V)V ref 42* – Fig. 9) to data inlined directly in at least one operand or opcode of said instructions (e.g. *V ref* 91, data *FFF3* – Fig. 9 – Note: memory holding place of opcode being inlined directly by a substituted value reads on data inlined directly in at least one operand or opcode),

so that said at least one reference to information in said constant pool is eliminated (e.g. *V/V (ref) 42, FFF3 47* – Fig. 9 – Note: constant FFF3 in address 47 created in line with FOO1 reads on eliminating reference V/V ref in the original constant pool address 42); and

a virtual machine implemented on a microprocessor (col. 1, lines 16-34; Fig. 1,18) wherein the virtual machine is capable of executing the sequence of instructions (*Loading and Execution control 120*, Fig. 14).

As per claims 78-79, 81-85, refer to corresponding rejections of claim 60-61, 63-68, respectively.

As per claim 86, Wilkinson discloses Java Card technology (col. 7, lines 42-55; *Java card* --col. 8, lines 41-50; Fig. 3).

As per claim 87, this claim includes the same limitations as in claim 69 and claim 74; hence is rejected using the corresponding rejections as set forth therein.

As per claims 89-94, these claims are rejected with the corresponding rejections as set forth in claims 63-65, 67-68, and 86, respectively.

As per claim 95, Wilkinson discloses a method for using an application software program including an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18), the method comprising:

receiving (*Integrated Circuit Card 10*, Fig. 2) the software program in a resource-constrained device (RCD) having a memory (Fig. 14; col. 7, lines 43-56; said instructions previously converted from one class file (e.g. col. 10, lines 30-47; Fig. 5,6);

said conversion transforming one reference of at least one instructions to information in a constant pool (e.g. *main (ref), (V)V ref 42* – Fig. 9) to data inlined directly in at least one operand or opcode of said instructions (e.g. *V ref* 91, data *FFF3* – Fig. 9 – Note: memory holding place of opcode being inlined directly by a substituted value reads on data inlined directly in at least one operand or opcode),

so that said at least one reference to information in said constant pool is eliminated (e.g. *V/V (ref) 42, FFF3 47* – Fig. 9 – Note: constant FFF3 in address 47 created in line with FOO1 reads on eliminating reference V/V ref in the original constant pool address 42); and

executing the sequence of instructions on the RCD (*Loading and Execution control 120*, Fig. 14; Fig .18).

As per claim 97, Wilkinson further discloses storing the sequence of instructions on the RCD (e.g. *Card ROM 140* -- Fig. 14).

As per claim 99, Wilkinson further discloses transforming constant pool indices in the received set of instructions to corresponding data values (col. 9, lines 25-41; Fig 9; col. 9, line 64 to col. 10, line 10).

As per claims 100-101, 103-108, refer to corresponding rejections of claims 60-61, 63-68, respectively.

As per claim 109, this claim incorporates the limitations of claim 95; and is rejected with the corresponding rejections as set forth in claim 95; and further comprises the limitation of comprising at least one composite instruction. However, this limitation has been addressed in claims 69 or 87.

As per claims 110-115, 117-122, refer to corresponding rejections of claims 96-101, 103-108, respectively.

As per claim 123, this is the apparatus claim corresponding to claim 95 above; and is rejected using the corresponding rejections as set forth therein.

As per claims 124-129, 131-136, refer to corresponding rejections of claims 96-101, 103-108, respectively.

As per claim 137, this is the apparatus claim corresponding to claim 109 above; and is rejected using the corresponding rejections as set forth therein.

As per claims 138-143, 145-150, refer to corresponding rejections of claims 96-101, 103-108, respectively.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 62, 70, 80, 88, 96, 98, 102, 116, 130, and 144 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilkinson et al., USPN: 6,308,317, as applied to claims 59, 69, 77, 87, 95, 109, 123 and 137 above; in view of Cowe et al., USPN: 5,825,407 (hereinafter Cowe).

As per claim 62, Wilkinson does not specify that such the RCD is an 16-bit processor architecture for executing the instructions even though Wilkinson suggests the possibility of operating with 8,16 or 32-bit microprocessor (col. 1, line 61 to col. 2, line 2) and operation in the RCD being performed on 16-bit integers (col. 9, lines 29-41). One of ordinary skill in the art at the time of the invention would recognize the need for implementing a architecture so that the instruction architecture can be handle either 8, 16 or 32 bit instruction architecture as suggested by Wilkinson. Cowe discloses implementing 8, 16, or 32 bit type processor architecture for a ASIC according to the well-known concept of making use of embedded processors such as evidenced by Wilkinson's ASIC in embedded applications when more sophisticated micro-controllers for larger data and speed capability are available on the market as mentioned by Cowe (col. 12, line 54 to col. 13, line 7) at the time the invention was made. Hence, it would have been obvious for an ordinary skill in the art at the time of the invention was made, to

implement a RCD or embedded processor based on an 16-bit architecture capability and apply that architecture to Wilkinson's small device (RCD) processor or micro-controller system because that would enable the RCD to perform more advanced, larger numerical data-intensive, e.g. 16-bit integer or floating point arithmetic or complicated type of instructions in the software applications needed in today's technology and also to ensure the cross-platform portability of the product of the time where processor architecture capable of handling larger bus size is becoming a standard in the internet as mentioned by Cowe and the suggested teachings by Wilkinson.

As per claim 70, refer to rationale of rejection in claim 62 above.

As per claim 80, refer to rationale of rejection in claim 62.

As per claim 88, refer to rationale of rejection in claim 62.

As per claims 96 and 98, Wilkinson further suggests retrieving security-related data over a communication network and the Internet (col. 3, lines 40-46); and discloses downloading of software onto the RDC (Fig. 1, 2; col. 3, line 60 to col. 4, line 8; col. 7, line 66 to col. 8, line 8); **but does not explicitly teach** accessing the software program to download onto the RDC from the a network (re claim 96) or Internet (re claim 98). Based on the method by Cowe as to use a embedded processor in a device for home use (see Fig. 14-15) and purported for accessing, retrieving, storing, and distributing software and application data over a network or Internet, it would have been obvious for one of ordinary skill in the art at the time the invention was made to add to Wilkinson's system the accessing of application programs over the Internet or network because this would improve the availability of program to load the RCD while enhancing the resource usage efficiency for enabling data distribution from the external source providing machines connecting the RCD in a network as mentioned by both Wilkinson and Cowe.

As per claim 102, refer to rationale of rejection in claim 62.

As per claim 116, refer to rationale of rejection in claim 62.

As per claim 130, refer to rationale of rejection in claim 62.

As per claim 144, refer to rationale of rejection in claim 62.

Response to Arguments

7. Applicant's arguments filed 11/14/2005 have been fully considered but they are not persuasive. Following are the reasons.

(A) As per claim 59, Applicants have submitted that Wilkinson fails to teach or suggest the inlined data as recited in claim 59, such as the inlining would eliminate the reference to any constant pool (Appl. Rmrks, pg. 19, 3rd para). In the claim, what is explicitly recited as 'at least one reference to information in said constant pool is eliminated' cannot be construed exactly as 'reference ... is eliminated because the data has been inlined and consequently, ... it is unnecessary to access any constant pool'. The cause-to-effect relationship between the inlined data as claimed and the elimination as above-stated is unclear from interpreting the claim. Broad and reasonable interpretation seems to have imparted a construction different from what appears to have been alleged by Applicants, and the specifics in Fig. 9 by Wilkinson have been mapped to such interpretation. The claim does not preclude what is now being used in the rejection (ref V/V becoming FOO1 + FFF3) to read on the 'reference to said constant pool' being eliminated. Indeed, Wilkinson teaches using another form of referencing instructions as inlined data (see Foo1 14 and FFFF3 15,) to replace the previous reference to an address location (ref 91, 92, address 42) in the constant pool; and such replacing of a previous address in this constant pool reads on such elimination. That is, 'said constant pool' reads on the very constant pool by Fig. 9

wherein the original reference (see ref 91, 92) has been substituted with the FOO1 and FFF3 being inlined as a new reference instruction (see Fig. 9). The 'reference to information ... is eliminated' limitation thus has been met, because that reference (combo ref 91, 92 of Fig. 9) no longer exists (reference ... eliminated) in light of the above substitution. The rejection has also pointed out what in the Fig. 9 reads on data inlined directly in an operand or opcode. Concerning Applicants' assertion that the inlined data is the reason why the reference to *any* constant pool is eliminated (e.g. 'it is unnecessary to access any constant pool'), this assertion is not clearly explicit from the claim. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

(B) Applicants have submitted that Wilkinson discloses that both ILOAD_X and ILOAD are single instructions, that 'ILOAD_X was translated into an ILOAD instruction' and that does not disclose a composite instruction and that executing ILOAD results in a single load operation being performed (Appl. Rmrks, pg. 20, bottom). The claim recites 'said instructions comprising ... one composite instruction' such that the composite instruction is 'generating a result functionally equivalent to a result ... resulting from sequential execution of two or more other instructions'. Wilkinson has met this by showing that the bytecodes being loaded do have a form of composite instruction the decomposition of which is to have it executed by the Virtual card (e.g. Fig. 7, such stack loading reads on *the operations on the current object)* and such decomposition into its code executing parts (as stored in stack) reads on *functionally equivalent to a result* (the loading result) from *sequential execution of two or more other instructions* (

instruction to load a opcode and instruction to load a operand); and this decomposition has been shown in the rejection. The composite instruction has been construed as 'generating a result generated by 'operations on said current object resulting from sequential execution of two or more other instructions'. Since ILOAD_X and the tandem ILOAD-and-integer X are distinct instructions, the ILOAD and the X loading being called upon to fulfill the result from the operation on the current object, the object being required stack data in the loading process by Wilkinson, the 'sequential execution of ... other instructions' as claimed has been met. For the result being 'functionally equivalent to a result ... generated by operations ... resulting from sequential execution ...', the whole limitation amounts to just a composite instruction having a execution result such that it is functionally equivalent to execution in sequence by the 2 loading as set forth above of ILOAD and X in fulfill the object of the stack. The very nature of a composite form like ILOAD_x entails that more than one instructions would be needed to implement its execution of stack object loading; otherwise Wilkinson would not go through the pain of providing the composing of this particular form as evidenced in Appendix D (this appendix has been borrowed from a continuation - US 2003/0023954 - of Wilkinson's instant invention, both sharing a same set of specifications). Thus, the claim again does not provide sufficient teaching as to overcome what is used from Wilkinson to meet the so-called composite instruction. Besides, the definition of a composite instruction has been construed not as a multiple instructions structure but merely an instruction that when executed would generate a result being functionally equivalent to a *resulting* from sequentially executing two or more instructions; and this has been explained above. The fact that those instructions are being replaced by the composite instructions has been mapped to the ILOAD_X (in the Java Card

environment) in view of the decomposing into its parts at stack resolution time in Wilkinson (see Appendix D of US 2003/0023954).

(C) Applicants have submitted that the claims 71-76, 77-79, 81-86, 87, 89-94, 96, 97, 99-101, 103-108, 109-115, 117-122, 123-129, 131-136, 137-143, 145-150 (Appl. Rmrks, pg. 21-23) distinguish over Wilkinson in view of the arguments and issue raised against Wilkinson in claim 59 or 69. These claims are still rejected because the arguments against the rejection of claims 59 and 69 are not persuasive.

The claims 59-150 will stand rejected as set forth in the Office Action.

Conclusion

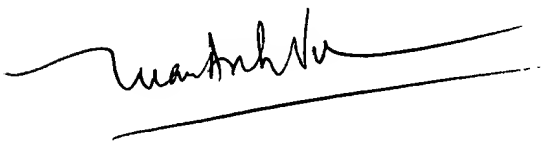
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan A Vu

Patent Examiner,
Art Unit 2193
December 17, 2005